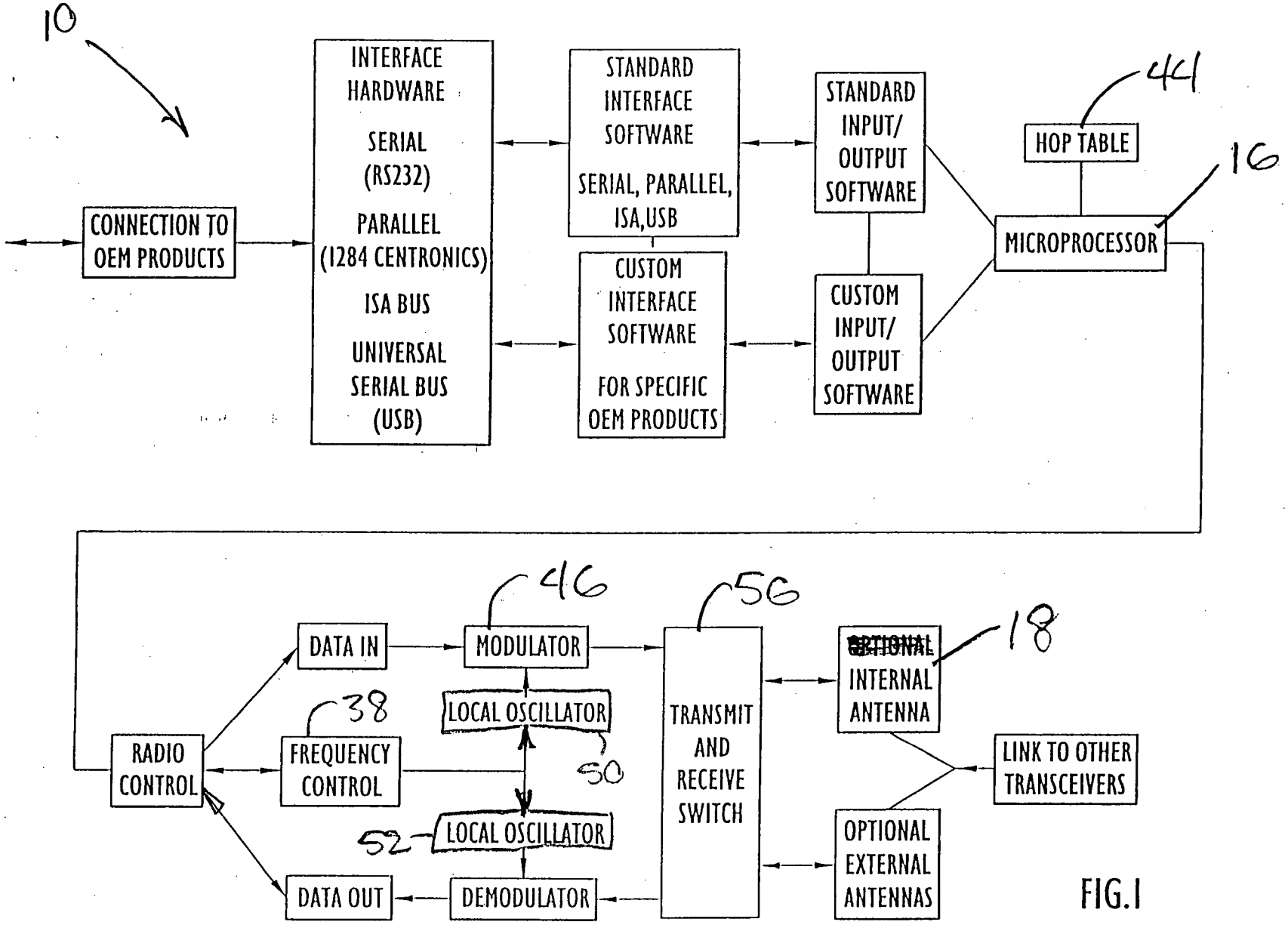


FIG.1

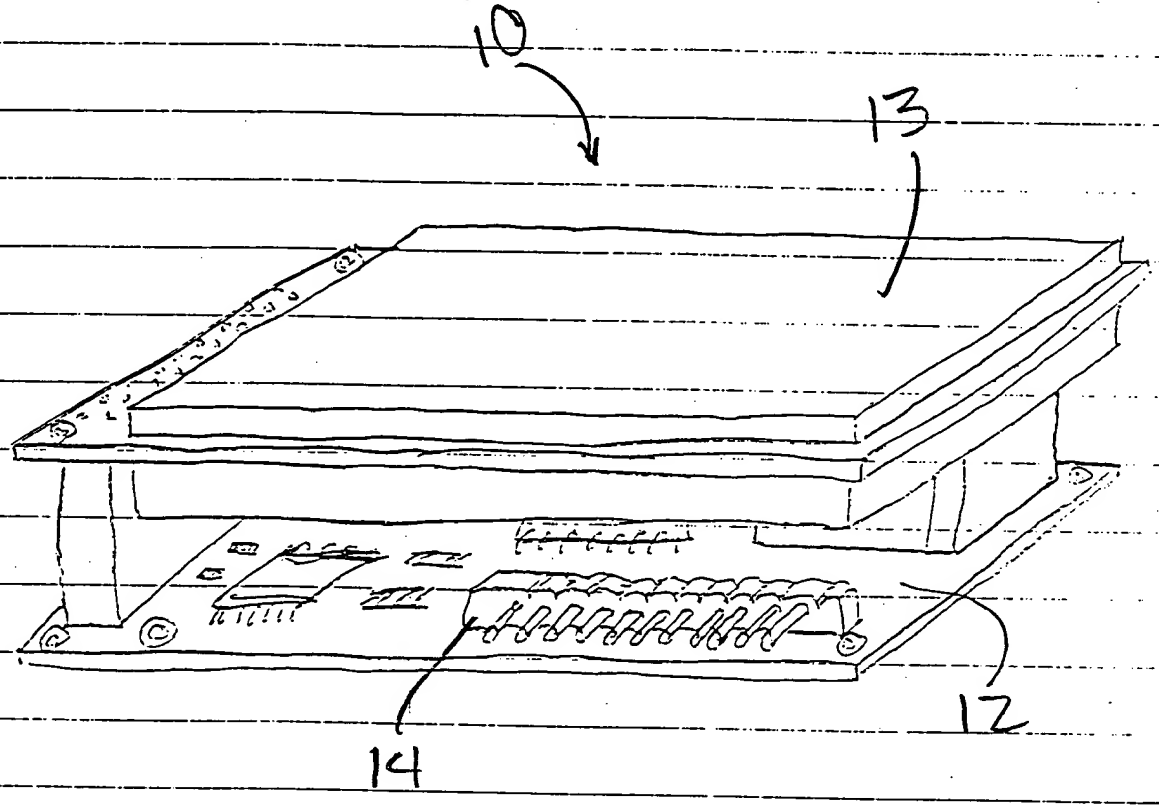


Fig. 2

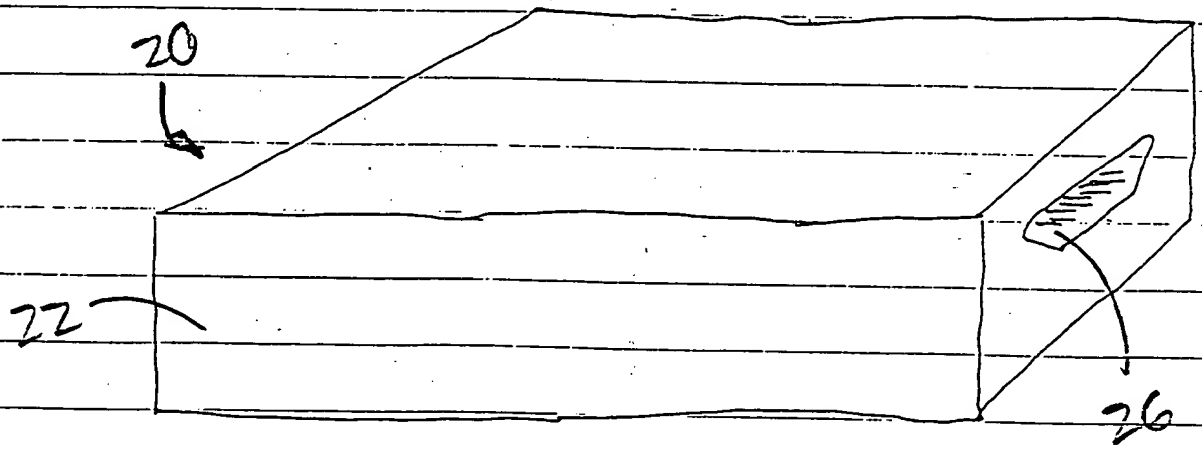


Fig. 3

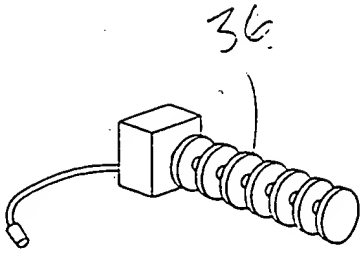


FIG.4A

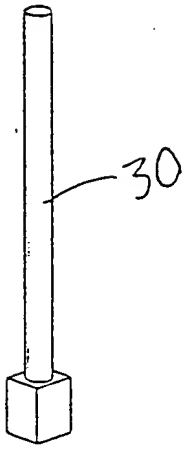


FIG.4B

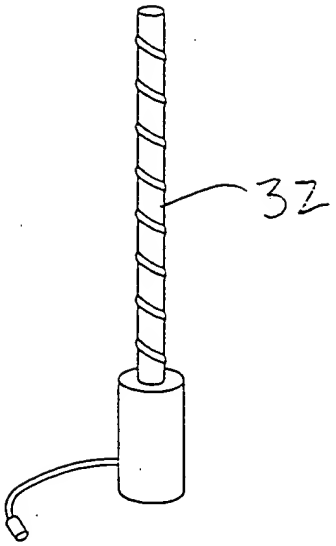


FIG.4C

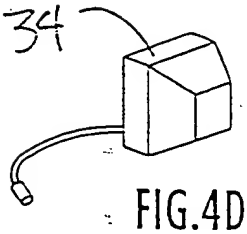


FIG.4D

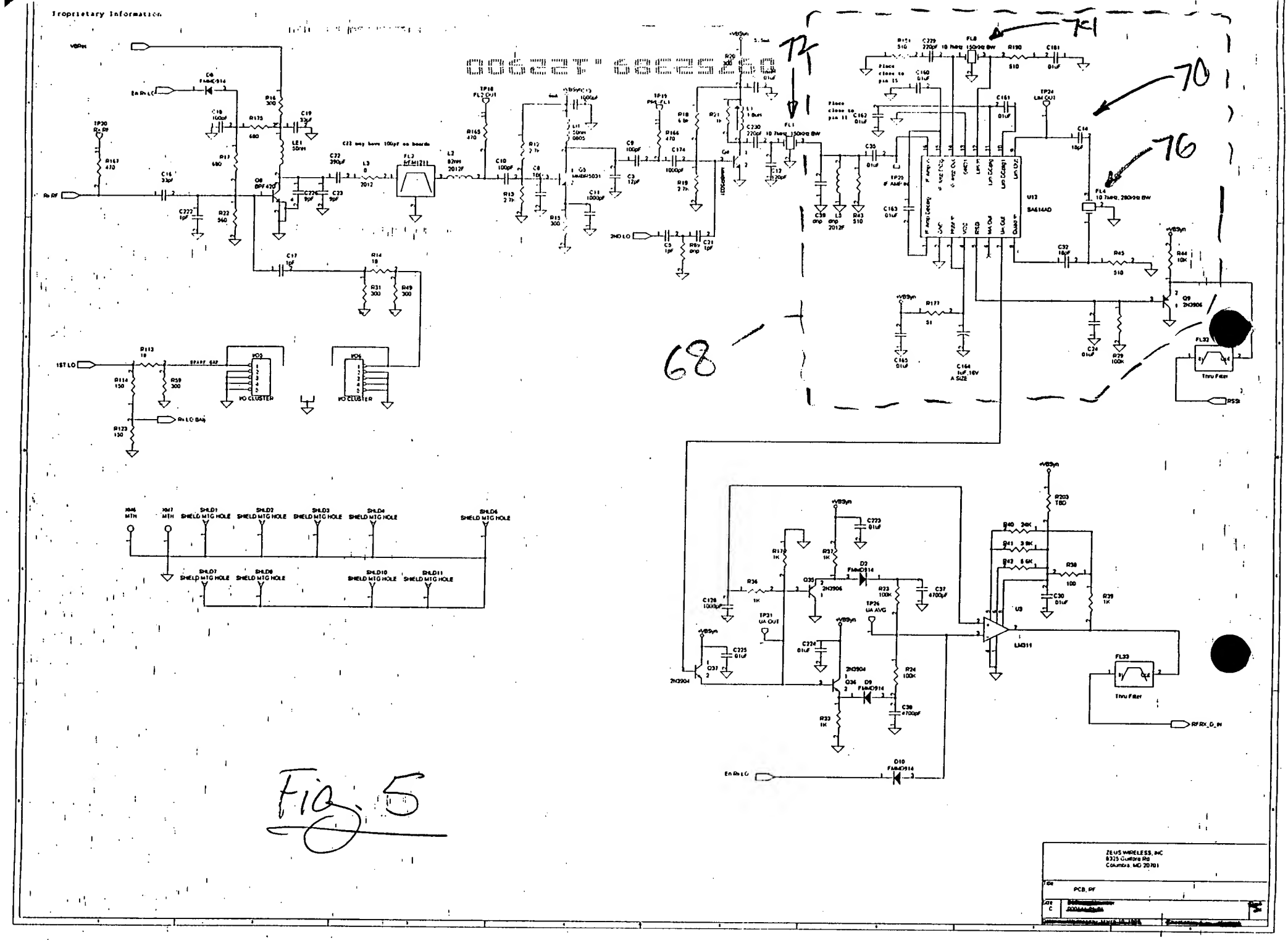


Fig. 5

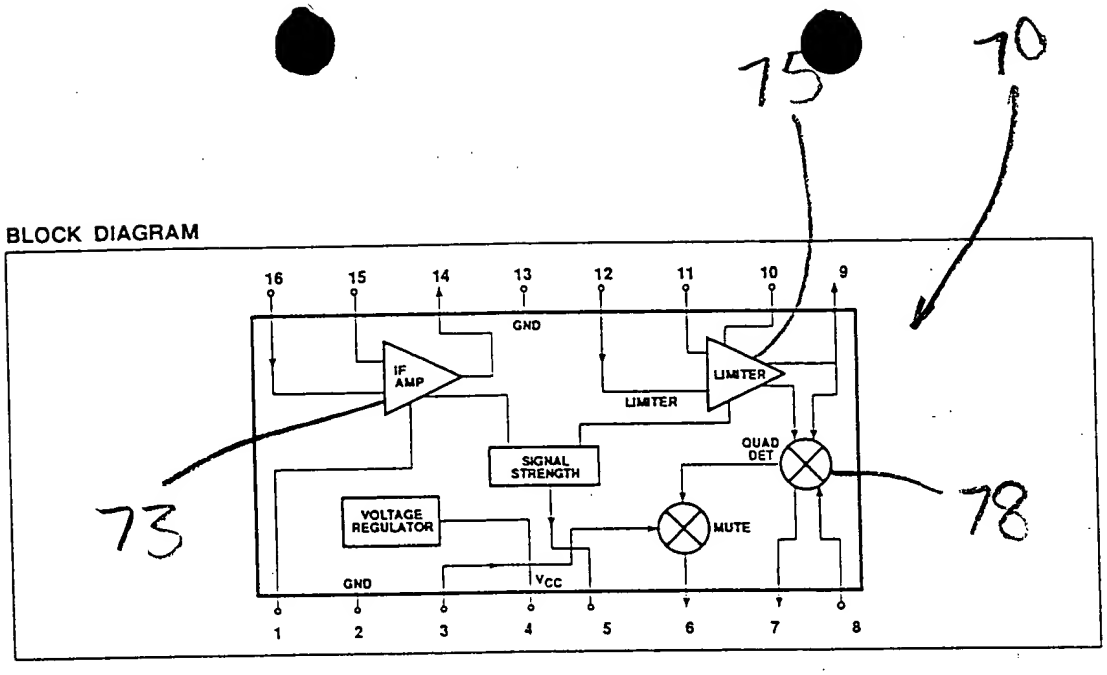
75
70
BLOCK DIAGRAM
16
15
14
13
12
11
10
9
GND
IF AMP
LIMITER
LIMITER
QUAD DET
SIGNAL STRENGTH
VOLTAGE REGULATOR
MUTE
GND
VCC
1
2
3
4
5
6
7
8
73
78

Fig. 6a

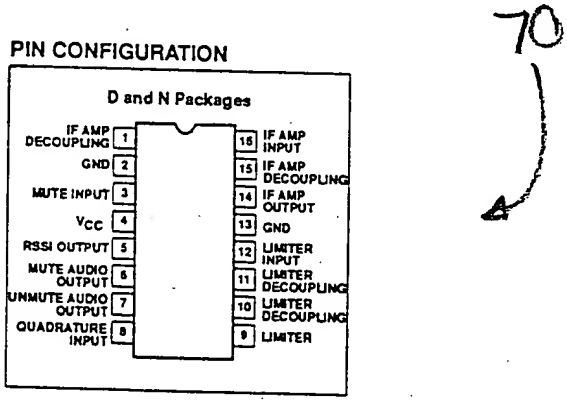
70
PIN CONFIGURATION
D and N Packages
IF AMP DECOUPLING 1
GND 2
MUTE INPUT 3
VCC 4
RSSI OUTPUT 5
MUTE AUDIO OUTPUT 6
UNMUTE AUDIO OUTPUT 7
QUADRATURE INPUT 8
16 IF AMP INPUT
15 IF AMP DECOUPLING
14 IF AMP OUTPUT
13 GND
12 LIMITER INPUT
11 LIMITER DECOUPLING
10 LIMITER DECOUPLING
9 LIMITER

Fig. 6b

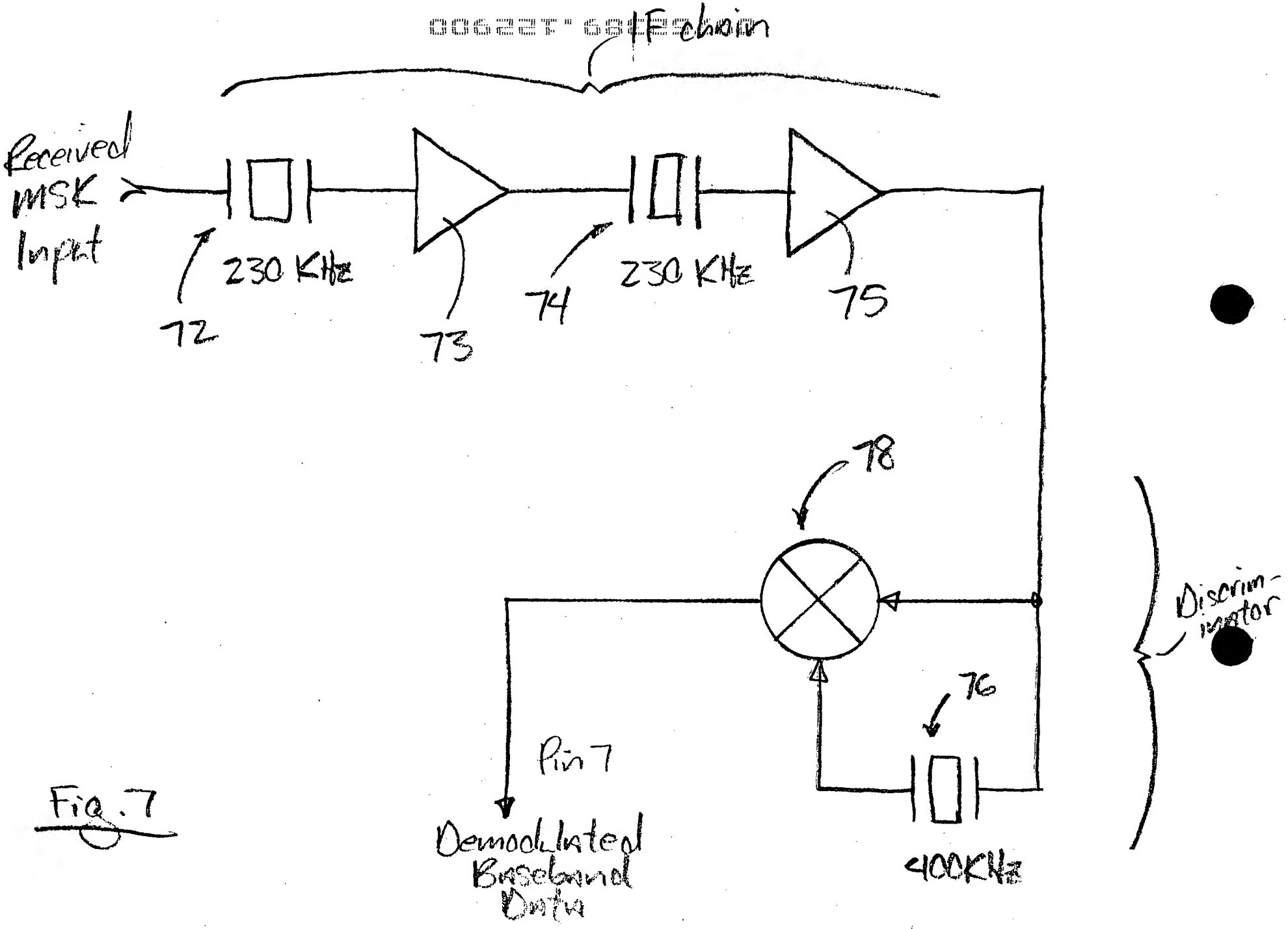
IF chain
Received MSK Input
230 KHz
230 KHz
72
73
74
75
78
76
400KHz
Discriminator
Pin 7
Demodulated Baseband Data

Fig. 7